A Review: CMOS Based Adders

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Abstract- Addition is representative of many arithmetic processing operations that must be carried out in portable digital systems, and the speed and power consumption trade-offs in adder hardware are of interest to portable digital system designers. Adders are commonly found in the critical path of many building blocks of Microprocessor and digital signal processor chips. A fast and accurate operation of digital system is greatly influenced by the performance of resident adders. Adders are key components in digital design; performing not only addition operations but also many other functions such as subtraction, multiplication and division. Adders of various bit-widths are frequently required in Very Large-scale Integrated Circuits (VLSI) from processors to Application specific Integrated Circuits (ASICs).In this paper different types of 8- bit adders are analyzed.

Index Terms: Carry select adder, carry increment adder, carry skip adder, carry look ahead adder.

I. INTRODUCTION

Adder is one of the most important components of a CPU (central processing unit). Fast adders are necessary in ALUs, for computing memory addresses, and in floating point calculations In addition, Full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors. Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are some of the most important cr iteria for the fabrication of DSP systems and high performance systems. The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing Modern Very Large Scale Integration (VLSI) circuits, low- power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the des ign of high- performance and low-power adders can be addressed at different levels , such as architecture, logic style, layout, and the process technology. The carry-ripple adder is composed of many cascaded single-bit full-adders. The circuit architecture is simple and area-efficient. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. The other types of adder circuits such as carry look- ahead adder, carry skip adder, carry select adder and carry increment adder are more complex than the conventional carry ripple adder and consume more power but these are very fast in operation. To quantify how effective or efficient a digital l design technology is in terms of delay and power; we use the product of the propagation delay and the power dissipation. To measure system efficiency we look at the power delay product of system.

II. CMOS Based ADDER ARCHITECTURES

Multiple-bit addition can be as simple as connecting several full adders in series or it can be more complex. How the full adders are connected or the technique that is used for adding multiple bits defines the adder architecture. Architecture is the most influential property on the computation time of an adder. This property can limit the overall performance. In general the computation time is proportional to the number of bits implemented in the adder. Many different adder architectures have been proposed to reduce or eliminate this proportional dependence on the number of bits. Several adder architectures are reviewed in the this section.

A. Ripple Carry Adder (RCA)

An n-bit r ipple carry adder consists of N full adders with the carry signal that ripples from one full-adder stage to the next, from LSB to MSB. It is possible to create a logical c ircuit using several full adders to add multiple-bit numbers. Each full adder inputs a Cin which is the Cout of the previous adder. Addition of k- bit numbers can be completed in k clock cycles. A N-bit ripple carry adder structures is shown in Fig. 1.

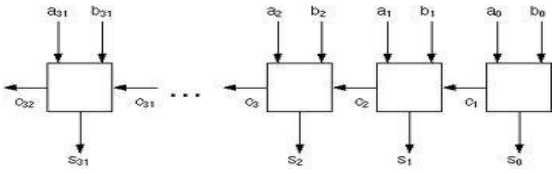

Fig. 1 N-bit Carry Ripple Adder

The ripple-carry adder has many advantages like low power consumption, low area and simple layout. The drawback of the ripple carry adder is its slow speed because each full adder must wait for the carry bit to be calculated from the previous full adder. Figure1.1 shows the CMOS based Ripple carry adder which is simulated in the EDA tool to calculate the statistics of the adder.

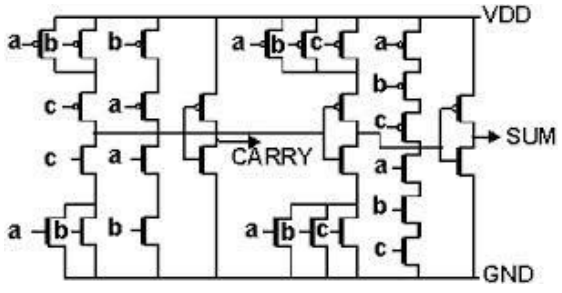

Fig 1.1 CMOS based Ripple carry adder

B. Carry Select Adder (CSA)

The carry select adder comes in the category of conditional sum adder. The carry select adder is constructed by sharing the common Boolean logic term in summation generation. To share the common Boolean logic term, only one XOR gate with one INV gate is needed to generate the summation signal pair as shown in Fig. 2. As the carry-in signal is ready, we can select the correct summation output according to the logic state of carry-in signal. As for the carry propagation path, we construct one OR gate and one AND gate to anticipate possible carry input values in advance. Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of carry-in signal. Figure 2.1 shows the CMOS based CSA which is s imulated in the EDA tool to calculate the statistics of the adder.

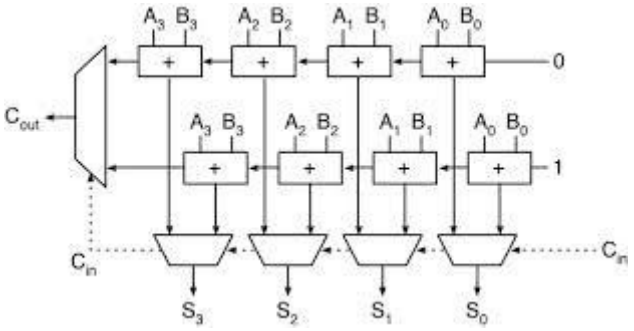

Fig. 2 Carry Select Adder

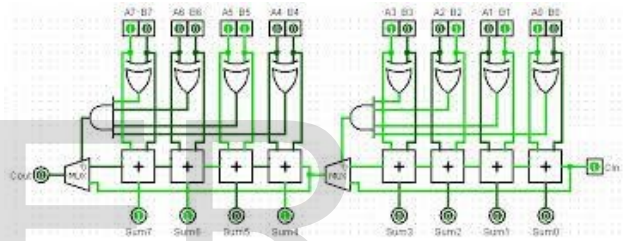

Fig 2.1 CMOS based Carry Select Adder

C. Carry Skip Adder (CSKA)

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder. The carry-skip adder is much like the RCA only it has a carry bypass path. This architecture divides the bits of the adder into an even number of stages M. Each stage M has a carry bypass path that forwards the carry-in of the Mi stage to the first carry-in of the Mi+1 stage. If the binary inputs are such that the carry would normally ripple (or propagate) from the input of the Mi stage to the input of the Mi+1 stage, then the carry takes the bypass path. The Carry Skip Adder reduces the delay

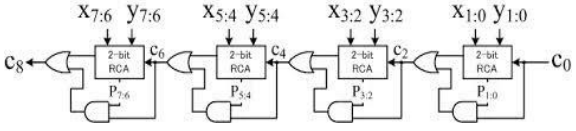

Fig. 3 Carry Skip Adder

due to the carry computation i.e. by skipping over groups of consecutive adder stages. Figure 3.1 shows the CMOS based Carry skip adder which is simulated in the EDA tool to calculate the statistics of the adder.

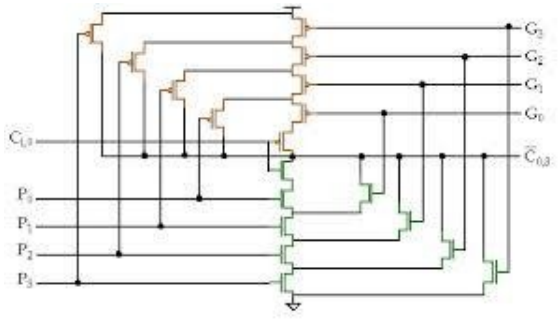

Fig 3.1 CMOS Carry Skip Adder

D. Carry Look -ahead Adder (CLA)

To reduce the computation time, faster way is to add two binary numbers by using carry look ahead adders. It is done by creating two signa ls (P and G) for each bit pos ition, based on if a carry is pr opagated through from a less signif icant bit pos ition (at least one input is a '1'), a carry is generated in that bit pos ition (both inputs are '1'), or if a carry is killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half- adder and G is the carry output of the same adder. After P and G are generated the carries for every bit pos ition are created.

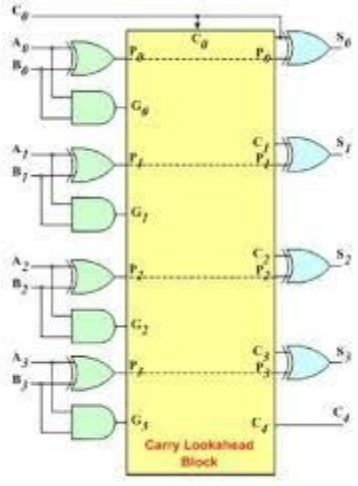

Fig. 4 Carry Look-ahead Adder

In carry look-ahead architecture instead of rippling the carry through a ll stages (bits) of the adder, it calculates all carries in parallel based on equation (2).

$$Ci = Gi + Pi.C\,i-1 \qquad (2)$$

In equation (2) the Gi and P i terms are defined as carry generate and carry propagate for the i^{th} bit. If carry generate is true then a carry is generated at the Ith bit. If carry propagate is true then the carry-in to the I^{th} bit is propagated to the carry-in of i+1 bit. They aredefined by equations (3) and (4) where Ai and Bi are the binary inputs being added.

$$Gi = Ai.Bi \qquad (3)$$
$$Pi = Ai + Bi \qquad (4)$$

Figure 4.1 shows the CMOS based Carry look ahead adder which is s imulated in the EDA tool to calculate the statistics of the adder.

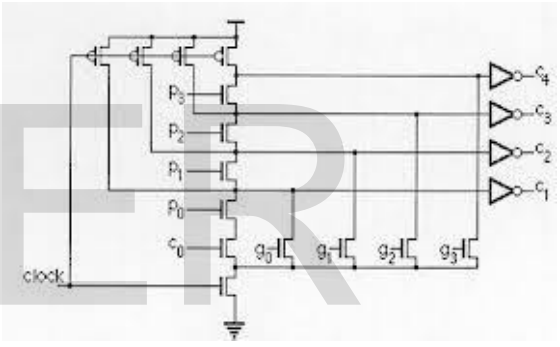

Fig 4.1 CMOS Carry Look-Ahead Adder

E. Carry Increment Adder (CIA)

In carry increment adder architecture instead of computing two results for each block and selecting the correct one, only one sum is calculated and incremented afterwards if necessary, according to the carry input. Thus the second adder and the multiplexers in the carry-select scheme can be replaced by a much smaller incrementer structure as shown in Fig.

5. Put differently, the computation of a second sum and carry bit is reduced to the generation of a propagate signa l per bit position.

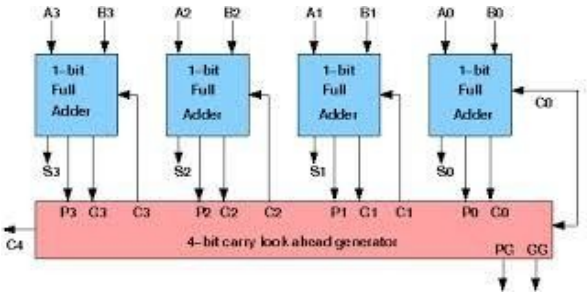

Fig. 5 Carry Increment Adder

Figure 5.1 shows the CMOS based CIA which is simulated in the EDA tool to calculate the statistics of the adder.

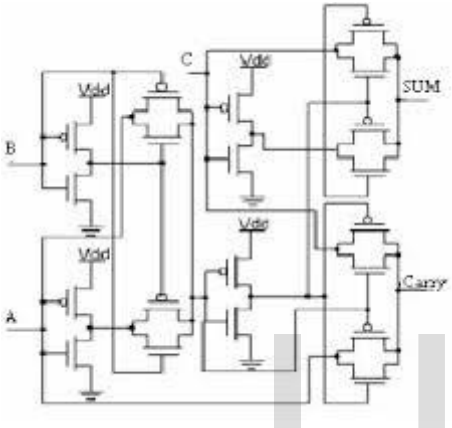

Fig 5.1 CMOS Carry Increment Adder

F. Carry Save Adder

A Carry-Save Adder is just a set of one-bit fulladders, without any carry-chaining. Therefore, an n-bit CSA receives three n-bit operands, name ly A(n-1)..A(0), B(n- 1)..B(0), and CIN(n-1)..CIN(0), and generates two n-bit result values, SUM(n-1)..SUM(0) and COUT(n-1)..COUT(0).

The most important application of a carry-save adder is to calculate the partial products in integer multiplication. This allows for architectures, where a tree of carry-save adders (a so called Wallace tree) is used to calculate the partial products very fast. One 'normal' adder is then used to add the last set of carry bits to the last partial products to give the final multiplication result. Usually, a very fast carry-look ahead or carry-select adder is used for this last stage, in order to obtain the optima l performance.

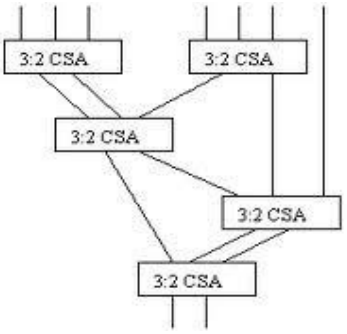

Fig 6. Carry Save Adder

Figure 6.1 shows the CMOS based carry save adder which is simulated in the EDA tool to calculate the statistics of the adder.

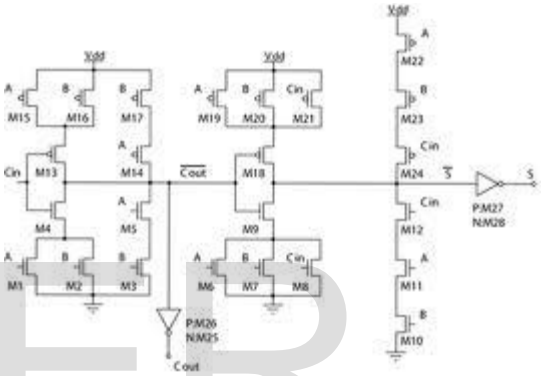

Fig 6.1 CMOS Based Carry Save Adder

G. Carry bypass Adder

The n-bit-carry-skip adder cons ists of a n-bit-carry-ripple-chain, a n- input AND-gate and one multiplexer. Each propagate bit , that is provided by the carry-ripple-chain is connected to the n-input AND-gate.

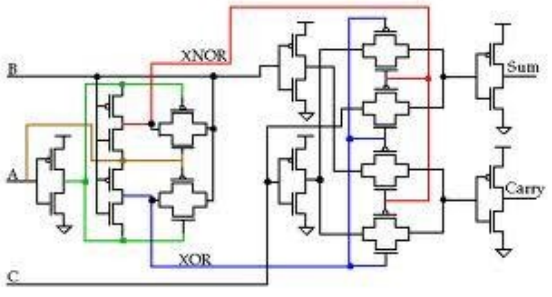

Fig 7.1CMOS Carry Skip Adder

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